REMARKS

Claims 16-20 were previously pending in this patent application. Claims 16-20 stand rejected. Herein, Claims 16 and 19 have been amended. Accordingly, after this Amendment and Response, Claims 16-20 remain pending in this patent application. Further examination and reconsideration in view of the amendments and arguments set forth below is respectfully requested.

Attached hereto is a marked-up version of the changes made to the patent application by the current amendment. The attached page is captioned "**Version With Markings To Show Changes Made.**"

35 U.S.C. Section 112, First Paragraph, Rejections

Claim 19 stands rejected under 35 U.S.C. Section 112, First paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. In particular, the Office Action states that the phrase "self-limiting diffusion process" is not supported by the description in the original disclosure.

Herein, Claim 19 has been amended so that the phrase "self-limiting diffusion process" is changed to "corner-limiting diffusion process". In view of the amendment to Claim 19, Applicants respectfully submit that Claim 19 contains subject matter which is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the

time the application was filed, had possession of the claimed invention, pursuant to 35 U.S.C. Section 112, First paragraph. Thus, Claim 19 is in condition for allowance.

35 U.S.C. Section 102(e) Rejections

Claims 16-18 stand rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al., U.S. Patent No. 6,127,226 (hereafter Lin). These rejections are respectfully traversed.

Independent Claim 16 recites:

> A method for fabricating a semiconductor device with a trenched gate comprising:
> etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;
> forming a trench-to-gate insulating layer inside the trench, ***wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench***;
> forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;
> forming a source region and a drain region in the semiconductor substrate ***such that the source and drain regions partially extend laterally underneath bottom of the trench***;
> forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and
> forming a control gate electrode on a top surface of the inter-gate dielectric layer. (emphasis added)

It is respectfully asserted that the teachings of Lin do not disclose the present invention as recited in Independent Claim 16. In particular, Lin is directed to a semiconductor memory device. In Lin, a tunnel oxide layer 23 is grown on the exposed surfaces of P doped sidewalls 22 and P doped bottom

surfaces 22 in trenches 20. [Lin, Col. 5, lines 37-41]. Moreover, an N+ S/D ion implantation is performed with a tilt angle θ=0 from the vertical to form the source/drain regions between the P doped sidewall regions 22. [Lin, Col. 5, lines 17-21]. Thus, the source/drain regions are formed between the P doped sidewall regions 22 and do not partially extend laterally underneath bottom of the trench 20.

Unlike Lin, Independent Claim 16 is directed to a method for fabricating a semiconductor device with a trenched gate, whereas the method includes etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate; forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench; and forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath bottom of the trench. While Lin describes growing a tunnel oxide layer 23 on the exposed surfaces of P doped sidewalls 22 and P doped bottom surfaces 22 in trenches 20, Independent Claim 16 recites the formation of a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench.

Moreover, while Lin requires an N+ S/D ion implantation to be performed with a tilt angle θ=0 from the vertical to form the source/drain regions between the P doped sidewall regions 22, Independent Claim 16 recites the formation of a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath bottom of the trench. Therefore, it is respectfully submitted that Independent Claim 16 is not anticipated by Lin and is in condition for allowance.

Dependent Claims 17-18 are dependent on allowable Independent Claim 16, which is allowable over Lin. Hence, it is respectfully submitted that Dependent Claims 17-18 are patentable over Lin for the reasons discussed above.

35 U.S.C. Section 103(a) Rejections

Claim 19 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent No. 6,127,226 (hereafter Lin) in view of Kroger, U.S. Patent No. 4,544,937 (hereafter Kroger). This rejection is respectfully traversed.

Dependent Claim 19 is dependent on allowable Independent Claim 16, which is allowable over Lin. Moreover, Kroger fails to teach a method for fabricating a semiconductor device with a trenched gate, whereas the method includes etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate; forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the

trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench; and forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath bottom of the trench, as recited in Claim 16. Hence, it is respectfully submitted that Dependent Claim 19 is patentable over Lin and Kroger for the reasons discussed above.

Claim 20 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., U.S. Patent No. 6,127,226 (hereafter Lin) in view of Wolf, U.S. Patent No. 3,873,371 (hereafter Wolf). This rejection is respectfully traversed.

Dependent Claim 20 is dependent on allowable Independent Claim 16, which is allowable over Lin. Moreover, Wolf fails to teach a method for fabricating a semiconductor device with a trenched gate, whereas the method includes etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate; forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench; and forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath bottom of the trench, as recited in Claim 16. Hence, it is respectfully submitted that Dependent Claim 20 is patentable over Lin and Wolf for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above amendments and remarks overcome all rejections. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 16-20) are now in condition for allowance.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present patent Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Version With Markings To Show Changes Made

IN THE CLAIMS

Claims 16 and 19 have been amended as follows:

16. (Once amended) A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

19. (Once amended) The method of claim 16 wherein the step of forming a ~~source region and a drain region comprises a [self-limiting]~~ corner limiting diffusion process.